51. (Amended) An integrated circuit comprising:

a semiconductive substrate;

a plurality of diffusion regions formed within the substrate, the diffusion regions and substrate forming junctions;

a plurality of conductive lines formed over the substrate and respective diffusion regions, the conductive lines having a generally uniform lateral width, and a portion of the conductive lines over the respective diffusion regions comprising an entirety of the lateral width of the conductive lines received directly over the respective diffusion regions, each conductive line comprising a pitch relative to an adjacent conductive line wherein the pitches are equal; and

wherein the junctions are configured to be reverse biased to preclude electrical shorting between the conductive lines and the substrate for selected magnitudes of current provided through the conductive lines.

52. (Amended) The integrated circuit of claim 51 wherein each diffusion region comprises a portion disposed outwardly from directly beneath respective conductive lines.

53. (Amended) The integrated circuit of claim 51 wherein each diffusion region comprises two portions disposed outwardly from directly beneath respective conductive lines.

54. (Amended) The integrated circuit of claim 51 wherein each diffusion region comprises two portions disposed outwardly from directly beneath respective conductive lines, a first portion outward of a first side of the conductive line and a second portion outward of a second side of the conductive line.

55. (Amended) An integrated circuit comprising:

a semiconductive substrate;

a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;

a conductive line formed over the substrate and the diffusion region, the conductive line comprising an entirety of a lateral width directly over the diffusion region;

a conductive material interconnecting the conductive line and the diffusion region, an entirety of the conductive material received directly over the diffusion region; and

wherein the diffusion region is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line.

56. The integrated circuit of claim 55 wherein the diffusion region comprises a portion disposed outwardly from directly beneath the conductive material.

57. The integrated circuit of claim 55 wherein the diffusion region comprises at least two portions disposed outwardly from directly beneath the conductive material.

58. The integrated circuit of claim 55 wherein the conductive material comprises metal.

59. (Amended) An integrated circuit comprising:

a semiconductive substrate;

a diffusion region formed within the substrate, the diffusion region and substrate forming a junction;

a conductive line formed over the substrate and the diffusion region;

a conductive material interconnecting the conductive line and the diffusion region, a portion of the conductive material received directly over the conductive line, and an entirety of the portion of the conductive material received directly over the diffusion region;

wherein the diffusion region is configured to be reverse biased to preclude electrical shorting between the conductive line and the substrate through the conductive material for selected magnitudes of current provided through the conductive line; and

wherein the diffusion region comprises at least two portions disposed outwardly from directly beneath the combined cross-sectional area of the conductive material and the conductive line.

60. Please cancel.

61. Please cancel.

D2 Subst Eq

62. The integrated circuit of claim 59 wherein the conductive material comprises metal.

Please add the following new claims:

**New Claims**

Subst Eq

63. (New) The integrated circuit of claim 51 wherein the conductive lines comprise substantially equal lateral widths.

D3

64. (New) The integrated circuit of claim 51 wherein the conductive lines comprise equal lateral spacing between adjacent conductive lines from a perspective defined by a plane generally parallel to an upper surface of the semiconductive substrate.

65. (New) The integrated circuit of claim 51 wherein the conductive lines comprise equal lateral spacing between adjacent conductive lines from a perspective defined by a plane generally parallel to an upper surface of the semiconductive substrate, and the lateral spacing substantially equals respective lateral widths of the conductive lines.

66. (New) The integrated circuit of claim 55 wherein the conductive line comprises at least two conductive layers.

67. (New) The integrated circuit of claim 55 wherein the conductive line comprises two conductive layers, one conductive layer directly over the other conductive layer.

68. (New) The integrated circuit of claim 55 wherein the conductive line comprises opposite sides extending from the semiconductive substrate, and further comprising sidewall spacers adjacent respective sides.

69. (New) The integrated circuit of claim 59 wherein the conductive line comprises at least two conductive layers.

70. (New) The integrated circuit of claim 59 wherein the conductive line comprises two conductive layers, one conductive layer directly over the other conductive layer.

71. (New) The integrated circuit of claim 59 wherein the conductive line comprises opposite sides extending from the semiconductive substrate, and further comprising sidewall spacers adjacent respective sides.